Data & signal protection
ESP PCB/D & PCB/TN Series

LPZ 0→3 | **FULL MODE** Bonding + Equipment Protection | **SIGNAL/ TELECOM** TEST CAT D + C + B | **ENHANCED** Low let-through voltage | **LOW IN-LINE RESISTANCE** 9.4 Ω | **CURRENT RATING** 300 mA

Combined Category D, C, B tested protector (to BS EN 61643) for 'through hole' mounting directly onto the PCB of data communication, signal or telephone equipment. Available for working voltages of up to 110 Volts. ESP PCB/TN suitable for Broadband, POTS, dial-up, T1/E1, lease line and *DSL telephone applications. For use at boundaries up to LPZ *0* to protect against flashover (typically the service entrance location) through to LPZ 3 to protect sensitive electronic equipment.

Features & benefits

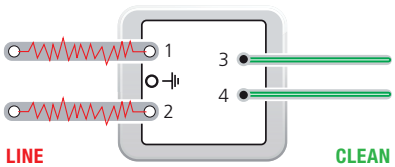
- Suitable for wave soldering
- Very low let-through voltage (enhanced protection to BS EN 62305) between all lines - Full Mode protection
- Full mode design capable of handling partial lightning currents as well as allowing continual operation of protected equipment
- Repeated protection in lightning intense environments
- Low in-line resistance minimises unnecessary reductions in signal strength
- 2 pin clean end and 3 pin line end to ensure correct insertion
- ESP PCB/TN is suitable for telecommunication applications in accordance with Telcordia and ANSI Standards (see Application Note AN005)

Installation

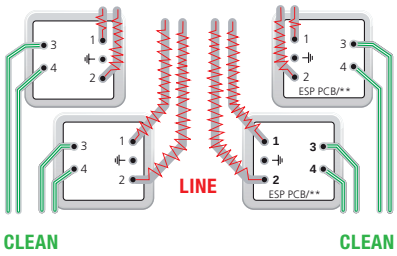
Connect in series, soldering pins direct onto PCB. Tracks to line and earth pins should be as wide as practical (see Furse Application Note AN003). Dirty (line) tracks should be routed parallel and as close together as possible. This should also be implemented on clean tracks, however clean tracks should never be routed close and parallel to line tracks or dirty barrier earth connections as transients can be re-introduced after the protector due to electromagnetic coupling.

The use of an earth layer or plane is highly recommended as this reduces the electromagnetic field produced by a transient discharging to earth considerably, and hence the chance of the transient being picked up on clean tracks.

Maximum line to clean separation. Large input tracks and pads (using top and bottom copper layers). Earth pin is bonded to an earth layer/plane.



All dirty (line) incoming tracks are separated from the clean output tracks, individual line and clean tracks are routed close together. Earth pins are bonded to an earth layer/plane.



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ESP PCB/D & PCB/TN Series - Technical specification

Electrical Specification	ESP PCB/06D	ESP PCB/15D	ESP PCB/30D	ESP PCB/50D	ESP PCB/110D	ESP PCB/TN
Nominal voltage[1]	6 V	15 V	30 V	50 V	110 V	–
Maximum working voltage *Uc*[2]	7.79 V	19 V	37.1 V	58 V	132 V	296 V
Current rating (signal)	300 mA					
In-line resistance (per line ±10%)	9.4 Ω	9.4 Ω	9.4 Ω	9.4 Ω	9.4 Ω	4.4 Ω
Bandwidth (-3 dB 50 Ω system)	800 kHz	2.5 MHz	4 MHz	6 MHz	9 MHz	20 MHz

Transient Specification		ESP PCB/06D	ESP PCB/15D	ESP PCB/30D	ESP PCB/50D	ESP PCB/110D	ESP PCB/TN
Let-through voltage (all conductors)[3] *Up*							
C2 test 4 kV 1.2/50 µs, 2 kA 8/20 µs to BS EN/EN/IEC 61643-21		12.0 V	25.0 V	44.0 V	78.0 V	155 V	395 V
C1 test 1 kV, 1.2/50 µs, 0.5 kA 8/20 µs to BS EN/EN/IEC 61643-21		11.5 V	24.5 V	43.5 V	76.0 V	150 V	390 V
B2 test 4 kV 10/700 µs to BS EN/EN/IEC 61643-21		10.0 V	23.0 V	42.5 V	73.0 V	145 V	298 V
5 kV, 10/700 µs[4]		10.5 V	23.8 V	43.4 V	74.9 V	150 V	300 V
Maximum surge current[5]							
D1 test 10/350 µs to	– Per signal wire	2.5 kA					
BS EN/EN/IEC 61643-21:	– Per pair	5 kA					
8/20 µs to ITU-T K.45:2003,	– Per signal wire	10 kA					
IEEE C62.41.2:2002:	– Per pair	20 kA					

Mechanical Specification	ESP PCB/D & PCB/TN Series
Temperature range	-40 to +80 °C
Connection type	0.64 mm (0.025") square PCB pins, 1.2 mm diameter PCB holes recommended
Case Material	ABS UL94 V-0
Dimensions	See diagram below

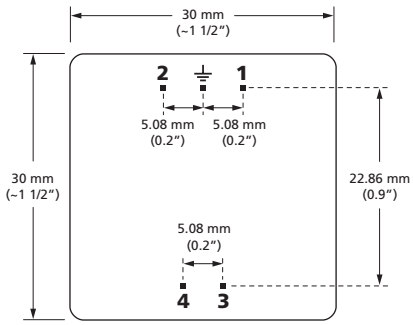
[1] Nominal voltage (DC or AC peak) measured at < 5 µA (ESP PCB/15D, ESP PCB/30D, ESP PCB/50D, ESP PCB/110D) and <200 µA (ESP PCB/06D)

[2] Maximum working voltage (DC or AC peak) measured at < 1 mA leakage (ESP PCB/15D, ESP PCB/30D, ESP PCB/50D, ESP PCB/110D), < 10 mA (ESP PCB/06D) and < 10 µA (ESP PCB/TN)

[3] The maximum transient voltage let-through of the protector throughout the test (±10%), line to line & line to earth, both polarities. Response time < 10 ns

[4] Test to IEC 61000-4-5:2006, ITU-T (formerly CCITT) K.20, K.21 and K.45,Telcordia GR-1089-CORE, Issue 2:2002, ANSI TIA/EIA/IS-968-A:2002 (formerly FCC Part 68)

[5] The installation and connections external to the protector may limit the capability of the protector



Depth: 20 mm (~0.8")
Weight: 35 g

Pins are positioned centrally
Pin 1 connects through Pin 3
Pin 2 connects through Pin 4

(Underside pin view)